Application No.: 10/650,010
First Inventor: Attila Kovacs
Title: SYSTEM AND METHOD FOR REDUCING TIMING VIOLATIONS DUE TO CROSSTALK IN AN INTEGRATED CIRCUIT DESIGN

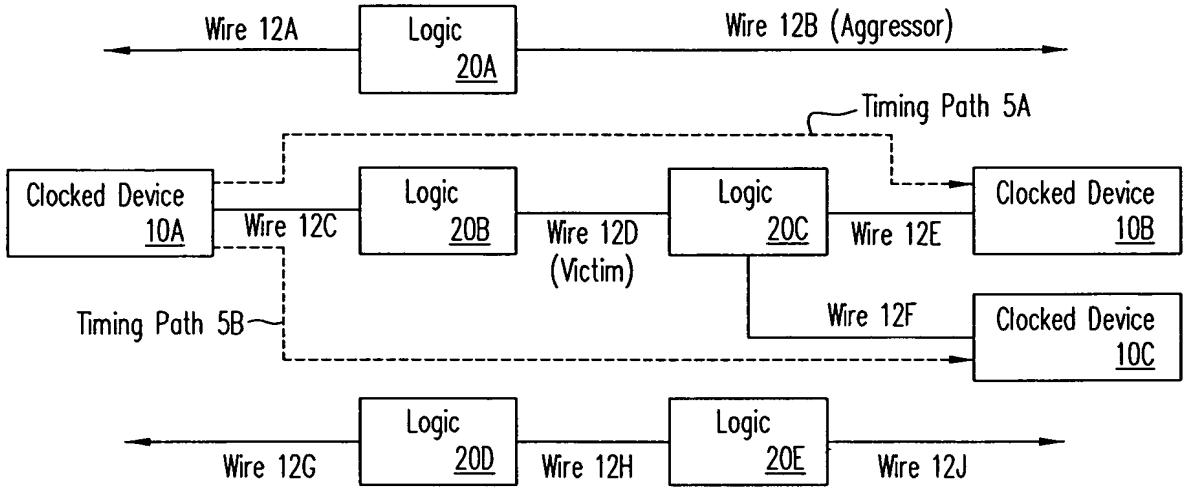

FIG. 1A

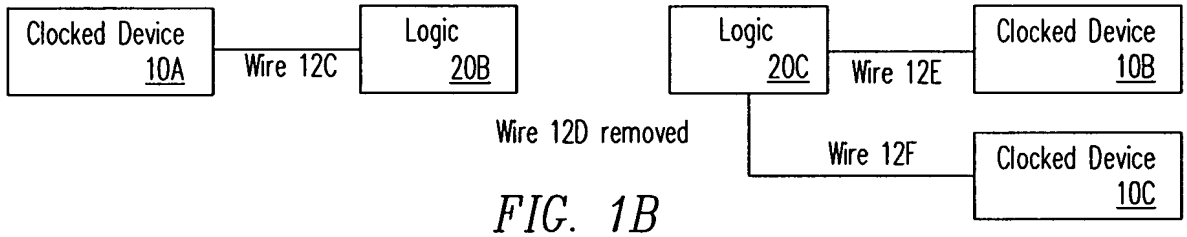

FIG. 1B

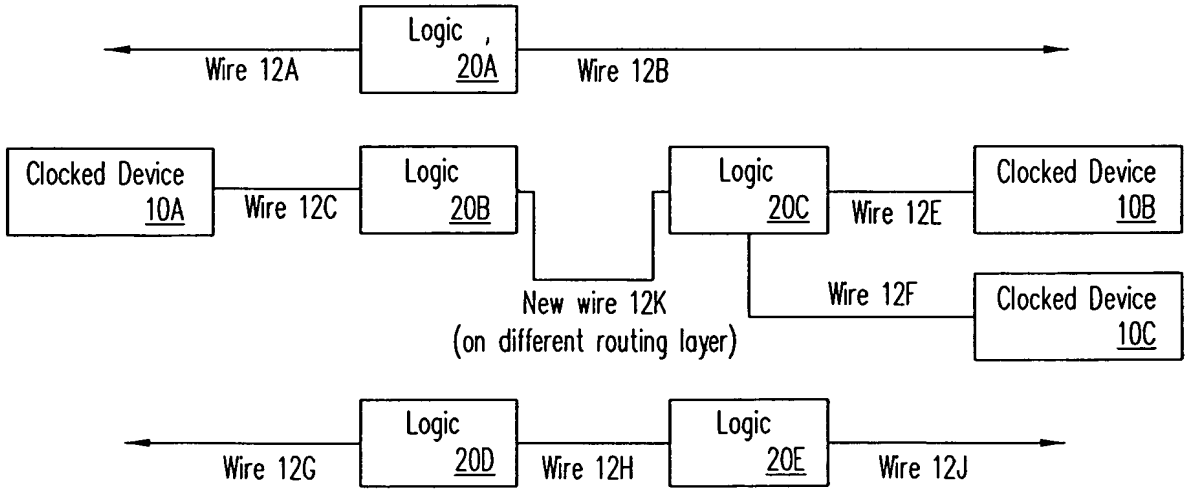

FIG. 1C

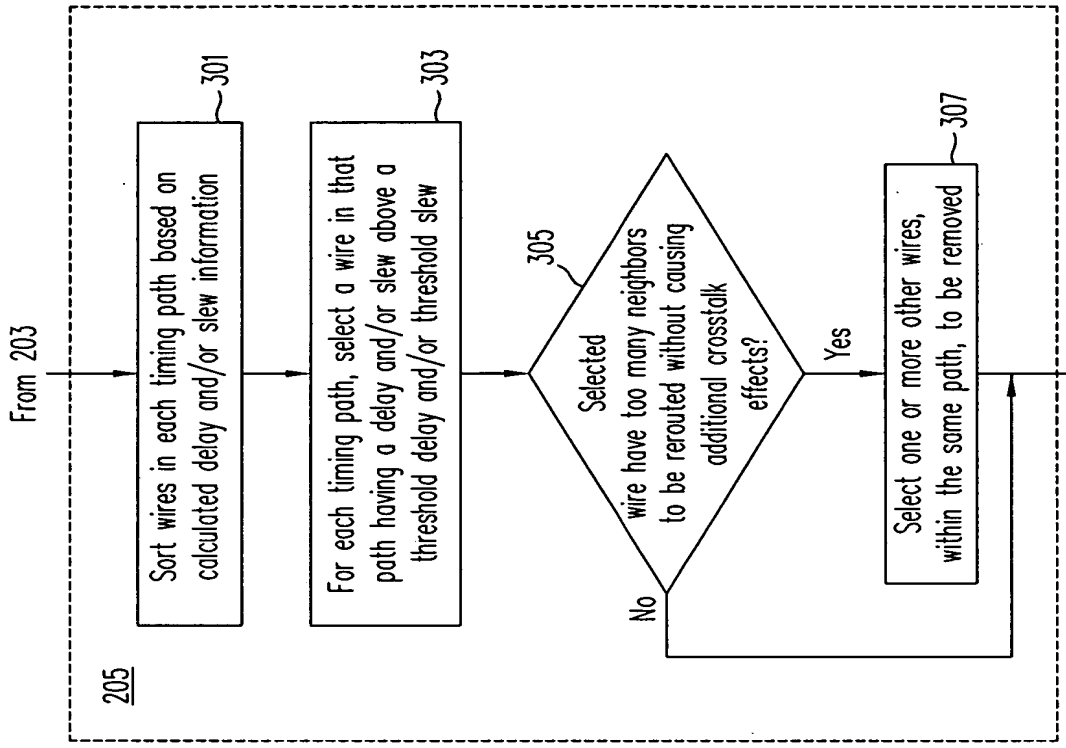
From 203
205
301
Sort wires in each timing path based on calculated delay and/or slew information
303
For each timing path, select a wire in that path having a delay and/or slew above a threshold delay and/or threshold slew
305
Selected wire have too many neighbors to be rerouted without causing additional crosstalk effects?
No
Yes
307
Select one or more other wires, within the same path, to be removed
To 207

FIG. 3

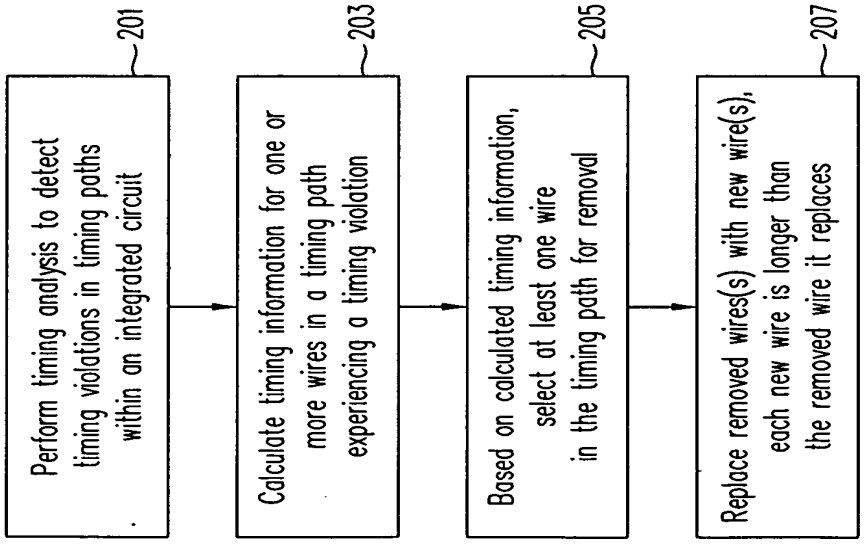
201
Perform timing analysis to detect timing violations in timing paths within an integrated circuit
203
Calculate timing information for one or more wires in a timing path experiencing a timing violation
205
Based on calculated timing information, select at least one wire in the timing path for removal
207
Replace removed wires(s) with new wire(s), each new wire is longer than the removed wire it replaces

FIG. 2

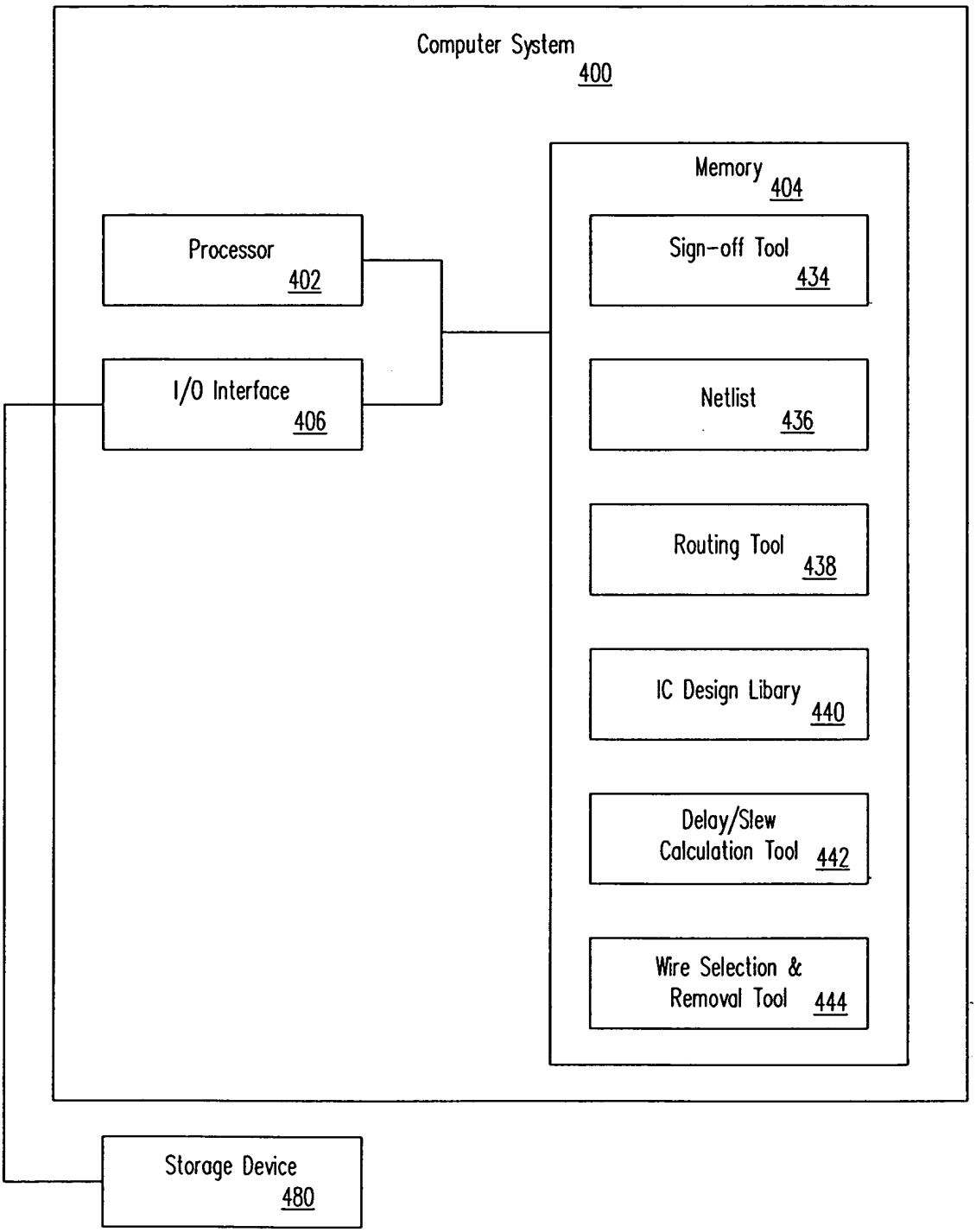
Computer System
400
Memory
404
Processor
402
I/O Interface
406
Sign-off Tool
434
Netlist
436
Routing Tool
438
IC Design Libary
440
Delay/Slew
Calculation Tool
442
Wire Selection &
Removal Tool
444
Storage Device
480

FIG. 4